ABSTRACT OF THE DISCLOSURE

A system of multiplexed data lines in a DRAM integrated circuit includes a switching circuit having two switching states. In one switching state, the data lines connect to a first configuration of data paths as would occur in a typical DRAM integrated circuit. A limited number of spare column select lines are available to repair defective column select lines in the first configuration. In another switching state, the data lines connect to a second configuration of the data paths, doubling the number of spare column select lines available to repair a defective column select line.